PRO-LOG CORPORATION

SUPPLEMENT TO VOLUMES I & II

July 1981

User's Manual

M980 CONTROL UNIT

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SUPPLEMENT TO
VOLUMES I AND II
M980 CONTROL UNIT USER'S MANUAL

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MISCELLANEOUS CORRECTIONS TO VOLUME I OF M980 USER'S MANUAL

PAGE	CORRECTIONS
i	Some of the referenced pages should be changed: FROM TO 5-17 5-21 5-2 5-3 5-6 5-5 5-8 5-9 5-11 5-13 5-13 5-15
V	Section 12 title should read: **BUFFER APPLICATIONS** Example 1 Page 12-1 Example 2 Page 12-2 Example 3 Page 12-3
5-23	Add note following first paragraph: "NOTE: Illegal Bit Check does not apply to gang modules. If an attempt is made to perform an Illegal Bit Check with a gang module, an 'E0' will be displayed."
6-15	Add note following first paragraph: "NOTE: Illegal Bit Check does not apply to gang modules. If an attempt is made to perform an illegal Bit Check with a gang module, an 'E0' will be displayed."
7-21	Under number 6, change the word "deleted" to read "affected". Under number 7, the display should read "1000".
9-1	Add to first paragraph: "Some gang modules may vary from these operations. See the individual operating instructions."

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MISCELLANEOUS CORRECTIONS TO VOLUME II OF M980 USER'S MANUAL

PAGE	CORRECTIONS
17-5	Under COMPARE operations, #5 should read: "Key in new format (01, 03, or 05) if desired."
18-3	Under "TTY OPERATING SEQUENCES (DATA ONLY) 9812-02" #5. delete "Asterisk(*),".
18-4	Under PROGRAM OPERATING SEQUENCE, #1: delete the word "listed" and replace with "programmed".
18-5	Under TTY ERRORS, second line from the bottom: delete "address field definition" and replace with "data transmission".
19-1	Photograph is incorrect. An M304 adapter is not needed to use the 9814 computer interface.
19-10	Figure 19-9 "Initialization": Each flow diagram should read as follows; START, SET INTERLOCK AND MODE ACTIVE, ADDRESS ACTIVE?, A. Change the note to read; NOTE: DEPRESS RESET AND KEY 4, OBSERVE 9814-00 IN DISPLAY,. Delete entire square "Set Mode Active."
20-3	Under 9818-00 "Remotely:" Add note: "After receiving the last data character the M980 will respond with a CR and LF".
20-6	Under 9818-06 LOCALLY: change ref. "page 20-7" to read "page 20-3". Under Locally: add note "After receiving the last data character the M980 responds with a CR and LF. Under 9818-10, first paragraph: change ref. "page 20-3" to read "page 20-7" delete "or via remote interface." Add note after title: "(4800 baud maximum)."
20-7	Under 9818-11 REMOTELY: add note: "No 'ACK' or 'NAK' is sent after receiving end-of-record." Under 9818-11, first paragraph: delete "or via remote interface". Under Remotely: add after "NAK" the words "and a CR,LF". Add note after title: "(4800 baud maximum)."

20-7 Under 9818-12, first paragraph: delete "or via remote interface". Add note after title: "(4800 baud maximum)."

20-9 Under 9818-16, first paragraph: delete "or via remote interface".

20-11 Under 9818-18, first paragraph: delete "or via remote interface".

20-12 The last sentence on this page should read:" Keying ENTER after the QXY or QXN command returns the M980 to the last active 9818 format.

20-14 In the second paragraph, after "MDS IOB" add "or M304 Adapter." Add note to figure 20-3 that a jumper can alternately be added between pins 4 and 5 of the M304 adapter.

20-15 The IC number and type referenced in the third paragraph of the "Baud Rate" section plus the addresses in the "Location" section of the table are for the MDS#230.

For the MDS#235, the IC number is A82 and the IC type is a 2732. The addresses for the MDS#235 are E89A (09A), E89B (09B), and E8A3 (0A3).

20-17 Under MOTOROLA EXORcisor II, fourth paragraph, following "...terminal.", add: "(See diagram below)".

Under MOTOROLA EXORcisor II, diagram shown beneath the fifth paragraph; add this note: The cable between the keyboard terminal and the M304 is the original cable sent with the MOTOROLA EXORcisor II. The cable between the M304 and the EXORcisor II is a cable with a male connector at one end and a female connector at the other end. The RC-18 cable from Pro-Log will provide this connection."

20-19 Under TEKTRONIX 8002A MDL, UPLOAD TO 8002A: Change #2 to read: "2. Using the instructions on page 20-3, select the address field to be uploaded from the M980 RAM Buffer."

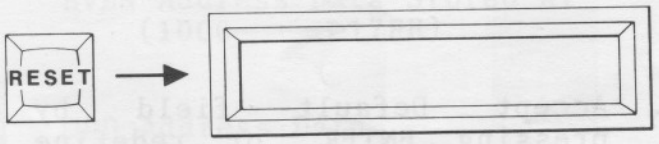
20-20 Under DTE AND DCE OPERATION, first paragraph, last line: replace "below" with "in Figure 20-7".

Buffer Edit - RAM Split

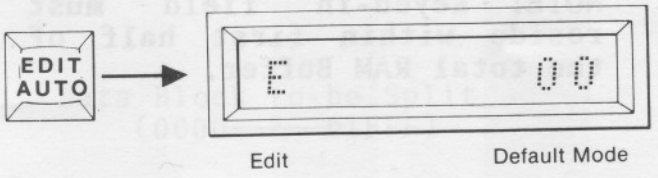
The RAM Split allows data stored anywhere in the first half of the RAM Buffer to be divided into two separate blocks. The two blocks always start at exactly half and three-quarters of the total RAM Buffer, respectively. The block starting at half of the total RAM contains the data originally resident at the start address and every other address in the block that is split. The block starting at three-quarters of the total RAM contains the start address plus 1, and every other address in the block that is split.

1. Select the switches as shown.

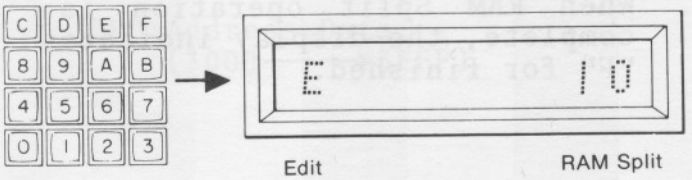
2. Depress RESET: The 8 hex displays are blank.



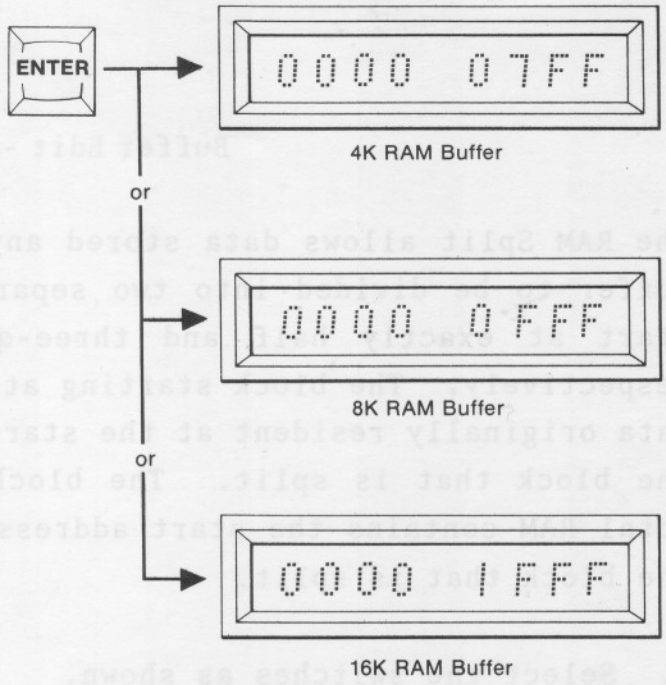
3. Depress EDIT: "E 00" is displayed to indicate Edit mode.



4. Using the hex keyboard, key in "10" to select the RAM Split mode.

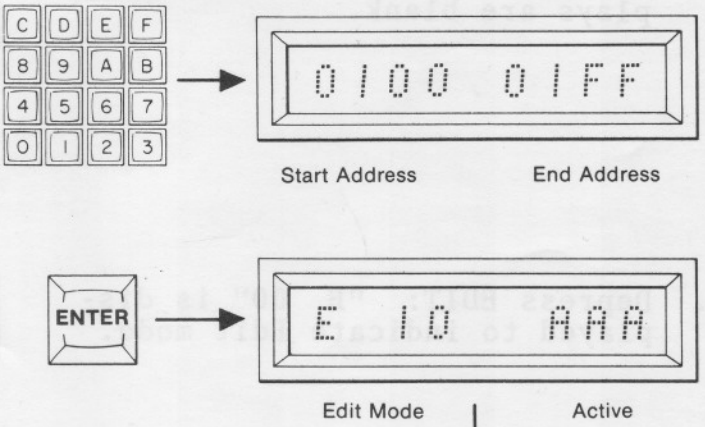


5. Depress ENTER. Display shows the Default Start and End Addresses of the RAM data field to be split. (Default size is one-half of Buffer size.)

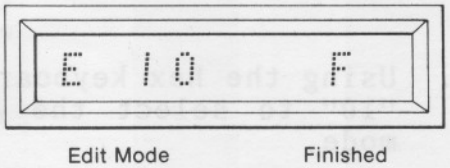


6. Accept Default field by pressing ENTER, or redefine using hex keyboard; then press ENTER to accept new field.

NOTE: Keyed-in field must reside within first half of the total RAM Buffer.

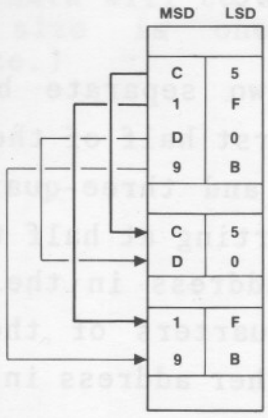


7. When RAM Split operation is complete, the display indicates "F" for finished.



8. RAM SPLIT EXAMPLES

a. 4K BUFFER EXAMPLE: (DEFAULT SIZE)



0000

Data Block to be Split
(0000 ⟶ 07FF)

07FF
0800

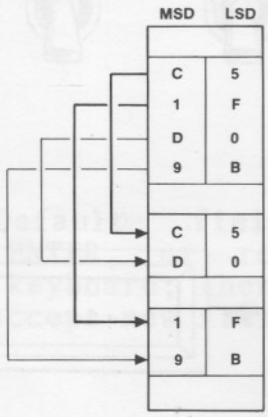
EVEN Address Data Stored at
(0800 ⟶ 0BFF)

0BFF
0C00

ODD Address Data Stored at
(0C00 ⟶ 0FFF)

0FFF

b. 8K BUFFER EXAMPLE: (DEFAULT SIZE)



0000

Data Block to be Split
(0000 ⟶ 0FFF)

0FFF
1000

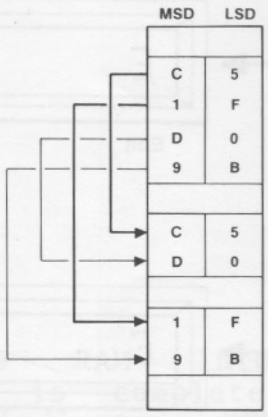
EVEN Address Data Stored at
(1000 ⟶ 17FF)

17FF
1800

ODD Address Data
(1800 ⟶ 1FFF)

1FFF

c. 16K BUFFER EXAMPLE: (DEFAULT SIZE)



0000

Data Block to be Split
(0000 ⟶ 1FFF)

1FFF
2000

EVEN Address Data
(2000 ⟶ 2FFF)

2FFF
3000

ODD Address Data
(3000 ⟶ 3FFF)

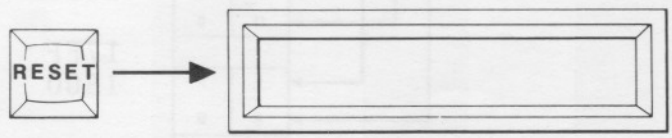
3FFF

Buffer Edit - RAM Interleave

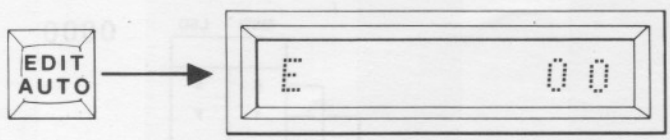
The RAM Interleave allows data stored in two separate blocks to be alternately stored in a defined area in the first half of the RAM Buffer. The two blocks always start at exactly half and three-quarters of the total RAM Buffer, respectively. The block starting at half the total RAM contains the start address and every other address in the block to be interleaved. The block starting at three-quarters of the total RAM, contains the start address plus 1, and every other address in the block to be interleaved.

1. Select the switches as shown.

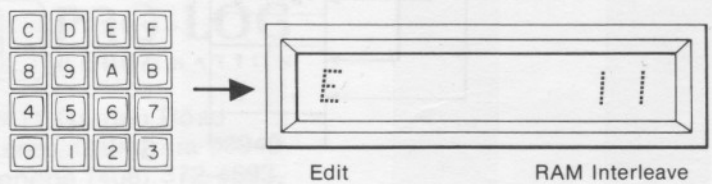
2. Depress RESET: The 8 hex displays are blank.



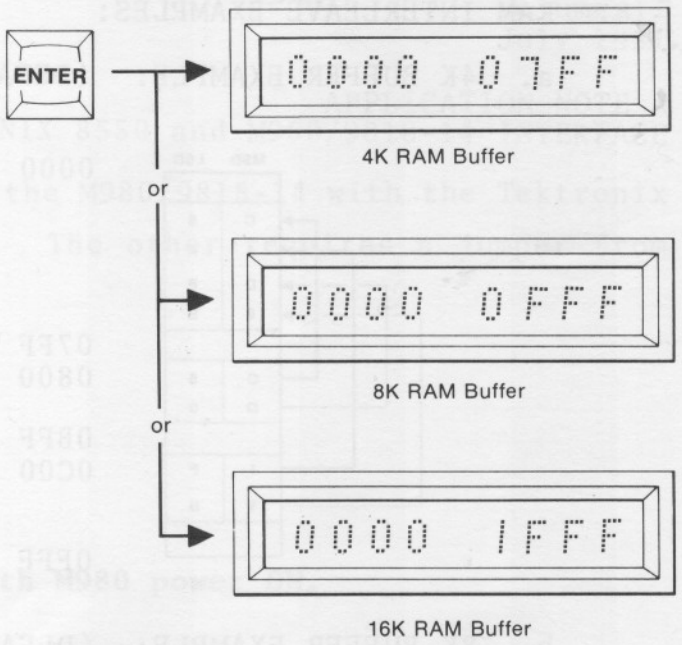
3. Depress EDIT: "E 00" is displayed to indicate Edit Mode.



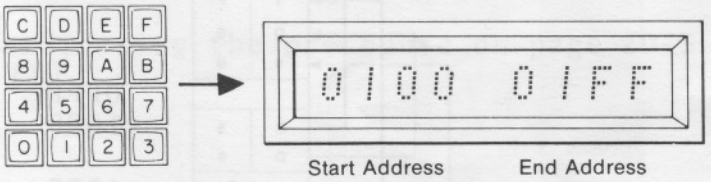
4. Using the hex keyboard, key in "11" to select the RAM Interleave mode.



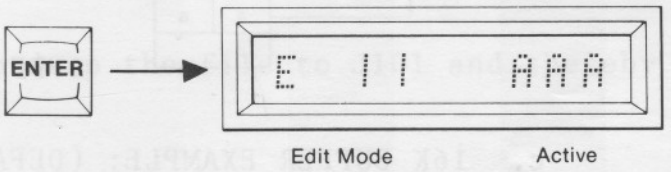
5. Depress ENTER. Display shows the Default start and end addresses of the RAM Buffer where the data will be stored. (Default size is one half Buffer size.)



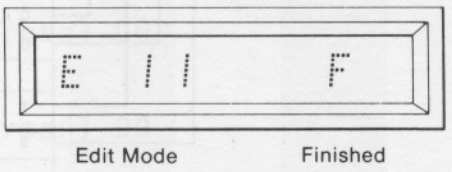
6. Accept Default field by pressing ENTER, or redefine using hex keyboard; then press ENTER to accept new field.



NOTE: Keyed-in field must reside within the first half of the total RAM Buffer.

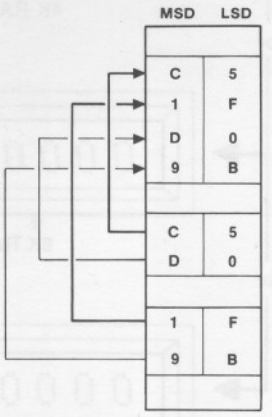


7. When the RAM Interleave operation is complete, the display indicates "F" for finished.



8. RAM INTERLEAVE EXAMPLES:

a. 4K BUFFER EXAMPLE: (DEFAULT SIZE)



0000

Data Block to Store Interleave Data
(0000 ⟶ 07FF)

07FF
0800

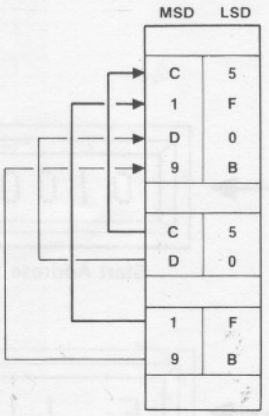
EVEN Address Data
(0800 ⟶ 0BFF)

0BFF
0C00

ODD Address Data
(0C00 ⟶ 0FFF)

0FFF

b. 8K BUFFER EXAMPLE: (DEFAULT SIZE)



0000

Data Block to Store Interleave Data
(0000 ⟶ 0FFF)

0FFF
1000

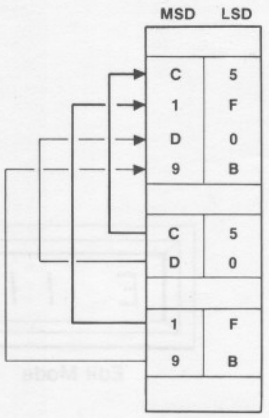
EVEN Address Data
(1000 ⟶ 17FF)

17FF
1800

ODD Address Data
(1800 ⟶ 1FFF)

1FFF

c. 16K BUFFER EXAMPLE: (DEFAULT SIZE)



0000

Data Block to Store Interleave Data
(0000 ⟶ 1FFF)

1FFF
2000

EVEN Address Data
(2000 ⟶ 2FFF)

2FFF
3000

ODD Address Data
(3000 ⟶ 3FFF)

3FFF

APPLICATION NOTE A
TEKTRONIX 8550 and M980/9818-14 INTERFACE

There are two methods for interfacing the M980/9818-14 with the Tektronix 8550. One requires no modifications. The other requires a jumper from pin 8 to pin 20 on the M304 adapter.

METHOD 1 (No Modifications)

Operating Sequence

NOTE: Do not install M304 adapter with M980 power ON.

1. Install M304 adapter in the parallel interface connector. Connect the terminal connector to J101 of the Tektronix 8550 DOS/50 via an RC-18 cable or equivalent.
2. Switch power on, and turn on the on-line modem switch.
3. Select 9818-14 via the hex keyboard, using the procedure on page 20-3 of the M980 User's Manual (Vol. II).

To Download to the M980 from the Tektronix 8550

The 8550 executes the WHEX command, to dump the file to J101 and thereby to the M980 RAM Buffer.

The 8550 is capable of downloading data to the M980 RAM Buffer in three formats. To dump in:

a. TEK HEX format, enter to the 8550:
   WHEX: REMO (Start Address)(End Address) 00

b. INTEL format, enter to the 8550:
   WHEX: I REMO (Start Address)(End Address) 00

c. MOTOROLA format, enter to the 8550:
   WHEX: M REMO (Start Address)(End Address) 00

Data in the program memory from the Start Address to the End Address, inclusive, transfers in the selected format to the M980 RAM Buffer, one line at a time (see "Address Offset" description, p. 20-3A). If a checksum error occurs, an "E6" is displayed. The M980 and 8550 must then be reset and the operation rerun. When the operation is completed, the 8550 prints the DOS/50 Prompt ( ).

To Upload to the Tektronix 8550 from the M980.

Execution of the RHEX command by the 8550, before a local list operation, initiates the upload operation.

1. The 8550 is capable of receiving data from the M980 RAM Buffer in three formats. To upload in:

   a. TEK HEX format, enter to the 8550:
      RHEX: REM1

   b. INTEL format, enter to the 8550:
      RHEX: I REM1

   c. MOTOROLA format, enter to the 8550:
      RHEX: M REM1

2. Key in Start and End Address, using the hex keyboard on the M980.

3. Depress ENTER.

The M980 outputs the RAM Buffer data located between the Start and End Addresses to the 8550's system memory, line by line in the selected format (see "Address Offset" description, p. 20-3A). When uploading is completed, the 8550 prints the DOS/50 Prompt ( ).

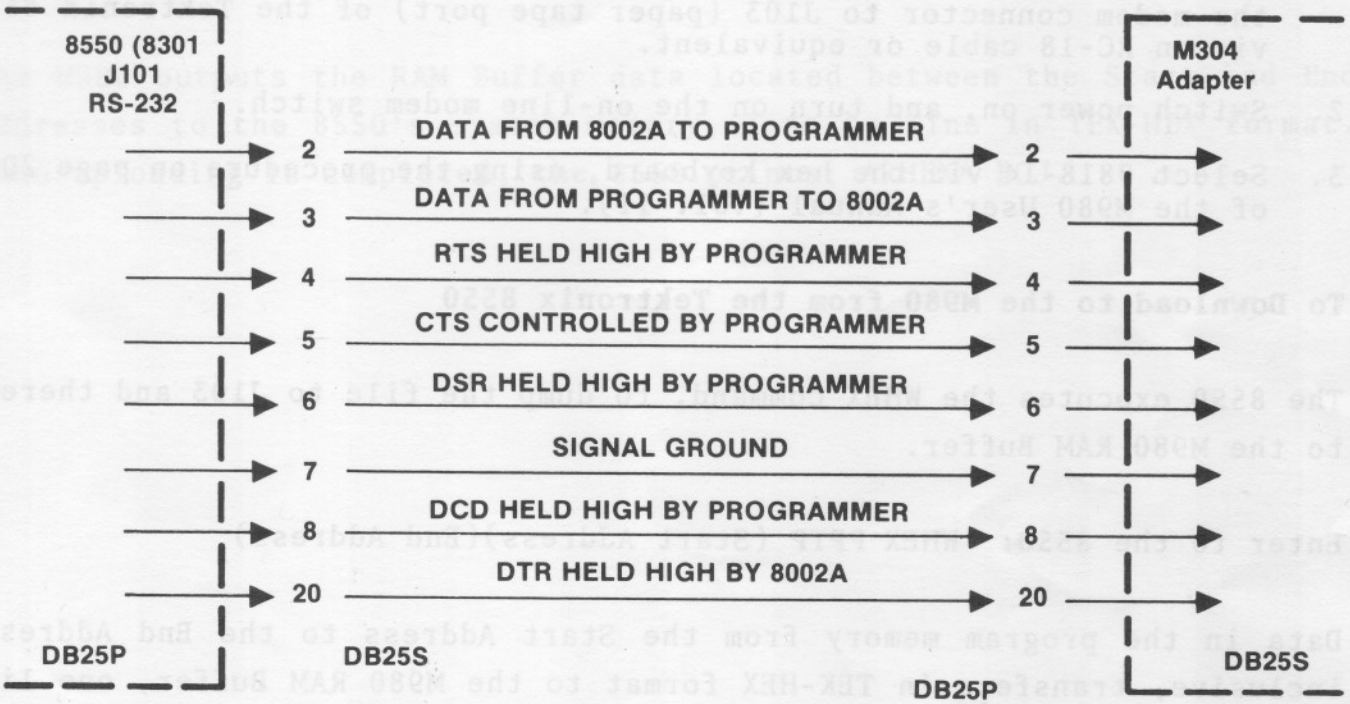


Figure A-1 M980/8550 Interconnect

METHOD 2 - (Modifications)

Operating Sequence

NOTE: Do not install M304 adapter with M980 power on.

1. Install M304 adapter in the parallel interface connector. Connect the modem connector to J103 (paper tape port) of the Tektronix 8550 via an RC-18 cable or equivalent.
2. Switch power on, and turn on the on-line modem switch.
3. Select 9818-14 via the hex keyboard, using the procedure on page 20-3 of the M980 User's Manual (Vol. II).

To Download to the M980 from the Tektronix 8550

The 8550 executes the WHEX command, to dump the file to J103 and thereby to the M980 RAM Buffer.

Enter to the 8550: WHEX PPTP (Start Address)(End Address)

Data in the program memory from the Start Address to the End Address, inclusive, transfers in TEK-HEX format to the M980 RAM Buffer, one line at a time. If a checksum error occurs, an "E6" is displayed. The M980 and 8550 must then be reset and the operation rerun. When the operation is completed, the 8550 prints: *WHEX* EOJ.

To Upload to the Tektronix 8550 from the M980

Execution of the RHEX command by the 8550, before a local list operation, initiates the upload operation.

1. Enter to the 8550: RHEX PPTR.
2. After selecting the 9818-14 active state on the M980, depress ENTER and key in the Start and End Addresses, using the hex keyboard.
3. Depress ENTER on the M980.

The M980 outputs the RAM Buffer data located between the Start and End Addresses to the 8550's system memory, line by line in TEK-HEX format. When uploading is completed, the 8550 prints: *RHEX* EOJ.

APPLICATION NOTE B
AMC SYSTEMS 8 & 29 INTERFACE WITH M980

When interfacing the M980 with AMC systems:

1. Use the M304 adapter and an RC-18 or equivalent cable.
2. Make sure that the AMC system has an RS-232C port available. Set the port for 4800 baud maximum, and even parity.
3. Connect the assigned AMC RS-232C port to the M304 modem connector, via the RS-232C cable.
4. Plug the M304 adapter into the parallel I/O connector on the M980.
5. Turn power on the M980 and the AMC system. **Note: Do not install M304 adapter while the M980 power is on.**
6. Place the M304 switches in the ON-LINE and MODEM ON positions.

To Download to the M980 RAM Buffer from AMC Systems 8 or 29

1. Determine the assigned RS-232C port name on the AMC system.
   Example: UPI:
2. On the M980, depress RESET, key 8, key 1, key 8, and ENTER.
   The M980 display shows "18 AAA".
3. Type on the AMC console: STAT PUN: = UPI:
   PIP PUN: = (file name to be downloaded)

The data stored in the file named is downloaded to the M980 RAM Buffer in the MOS TECH format. The left-most display on the M980 flashes "1" while the transfer is taking place. When completed, the M980 display shows "18 AAA".

To Upload to AMC System 8 or 9 from the M980 RAM Buffer

1. Determine the assigned RS-232C port name on the AMC system.
   Example: URI:

2. Type on the AMC console: STAT RDR: = URI:
   PIP (file name) = RDR:

3. On the M980, depress RESET, key 8, key 1, key 2, ENTER, and ENTER. The M980 display shows the Start and End addresses of the M980 RAM Buffer. Depress ENTER to upload the entire contents of the RAM Buffer or, using the M980 keyboard, key in the Start and End Addresses of the data you wish to upload to the AMC system. Depress ENTER.

The data stored between the previously selected Start and End addresses of the M980 RAM Buffer is transferred to the AMC system in the INTEL HEX format. (This format sends a "Control Z" character, which is required by the AMC system to terminate a transfer.) The left-most display on the M980 flashes "0" while the transfer is taking place. When completed, the M980 display will show "12 AAA".

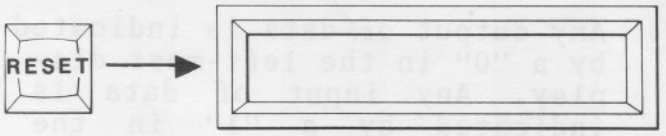
RS-232C FORMAT SELECTION (With Address Offset)

This sequence allows the substitution of a Default Address for the First Address received or listed. The Address Offset is automatically determined by the M980 and is subtracted from, or added to, all addresses in the Receive and List modes until the M980 is reset and a new Default Address is selected.

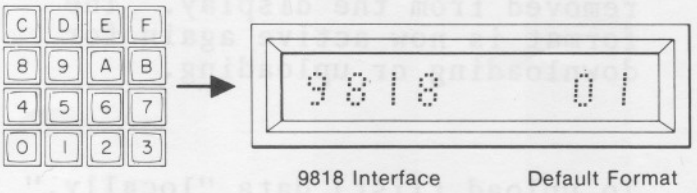
Operation

1. Install the M304 adapter on the M980 (power must be off), using RC-18 cable or equivalent. Connect to system via M304 terminal or modem connector, whichever is appropriate. Turn the M304 on-line switch on and modem on if attached. Select the switches as shown.

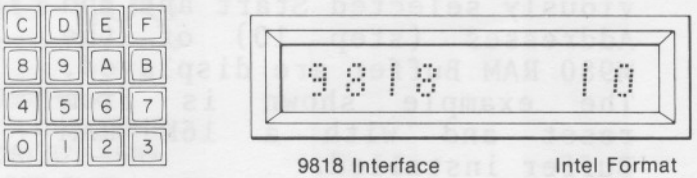
2. Turn M980 power on. Depress RESET. The 8 hex displays are blank.



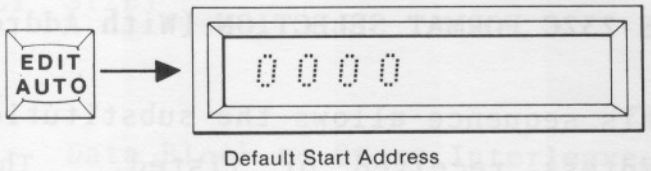
3. Depress key 8 to select the 9818 RS-232C option. Display shows "9818 01" as a Default format.



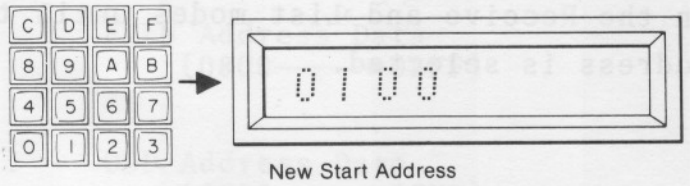
4. Select a new format using hex key pad. 9818-10 Intel format is shown. **Note: If an "E5" is displayed, check that the CTS and/or DTR lines are in the active (high) state.**



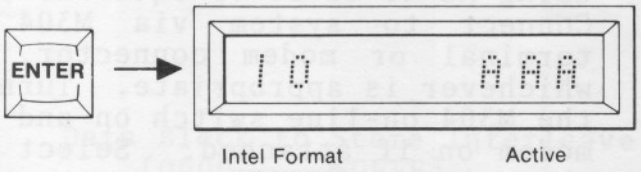
5. Depress the EDIT key to accept the selected format. The display shows "0000" to indicate the Default Start Address (explained later).



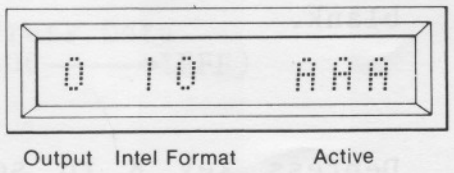
6. If a different Default Start Address is desired, use the hex key pad to enter the four-digit address. The example shown uses address "0100" as the Default Address (explained later).

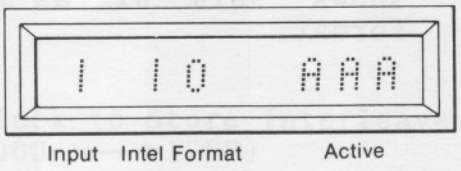


7. Depress ENTER. The Default Start Address is accepted. Display shows the selected format is now active for downloading (receiving) or remotely uploading (listing) the M980 Buffer data.

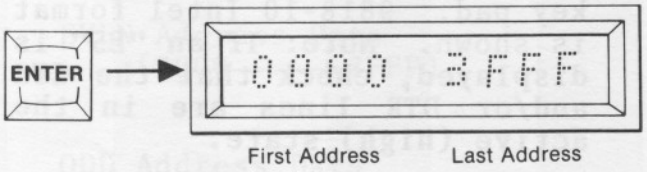


8. Any output of data is indicated by a "0" in the left-most display. Any input of data is indicated by a "1" in the left-most display. Upon completion, the "0" or "1" is removed from the display. The format is now active again for downloading or uploading.

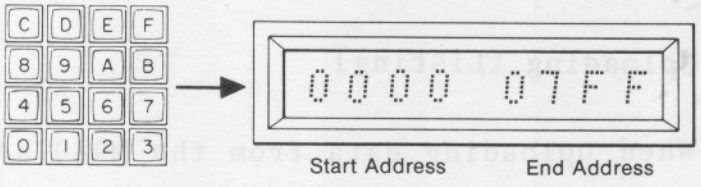




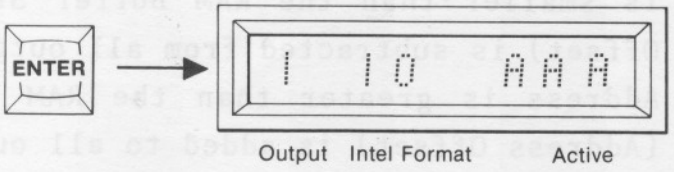
9. To upload (list) data "locally," depress ENTER. The First and Last Addresses or the previously selected Start and End Addresses (step 10) of the M980 RAM Buffer are displayed. The example shown is from reset and with a 16K RAM Buffer installed.



10. To upload a limited address field, key in new Start and End Addresses, using the hex keys.



11. Depress ENTER. The data located between the previously displayed addresses are uploaded to the remote source, in the selected format. A "0" is displayed in the left-most display as described in step 8.



Downloading (Receiving)

The Default Start Address "0000", or the entered Default Start Address (step 6), is compared to the First Incomming Address. If the Default Start Address is smaller than the First Incomming Address, the difference (Address Offset) is subtracted from all incomming addresses. If the Default Start Address is greater than the First Incomming Addresses, the difference (Address Offset) is added to all incomming addresses. The result of this addition or subtraction is then used as the Absolute Address of the RAM Buffer.

EXAMPLE: Using the Intel format 9818-10, the Default Start Address (step 6) is "0100". The incomming addresses are between "E000" and "FFFF". (See figure 20-3E.)

```
  E000 = First Address received.
- 0100 = Default Start Address.
  DF00 = Address Offset

  E000 = First Address received
- DF00 = Address Offset.
  0100 = Absolute Address of RAM Buffer

  FFF0 = Last Address received.
- DF00 = Address Offset.
  20F0 = Absolute Address of RAM Buffer.
```

Note: If an upload is performed after a download and before reset, the same address offset is used. This allows outgoing addresses to match incoming addresses without reinitializing a Default Address.

Uploading (Listing)

When uploading data from the M980 RAM Buffer, the Default Start Address is compared to the RAM Buffer Start Address. If the Default Start Address is smaller than the RAM Buffer Start Address, the difference (Address Offset) is subtracted from all outgoing addresses. If the Default Start Address is greater than the RAM Buffer Start Address, the difference (Address Offset) is added to all outgoing addresses. The result of this subtraction or addition is then used as the Absolute Address to be sent.

EXAMPLE: Using the Intel format 9819-10, the Default Start Address (step 6) is "E000". The RAM Buffer Start and End Addresses (step 9) are "0100" and "20FF", respectively. (See figure 20-3E.)

```
  E000 = Default Address
- 0100 = First (Start) Address of RAM Buffer.
  DF00 = Address Offset.

  0100 = First Address of RAM Buffer to be sent
+ DF00 = Address Offset.
  E000 = First Absolute Address sent.

  20F0 = Last Address of RAM Buffer to be sent.
+ DF00 = Address Offset
  FFF0 = Last Absolute Address sent.
```

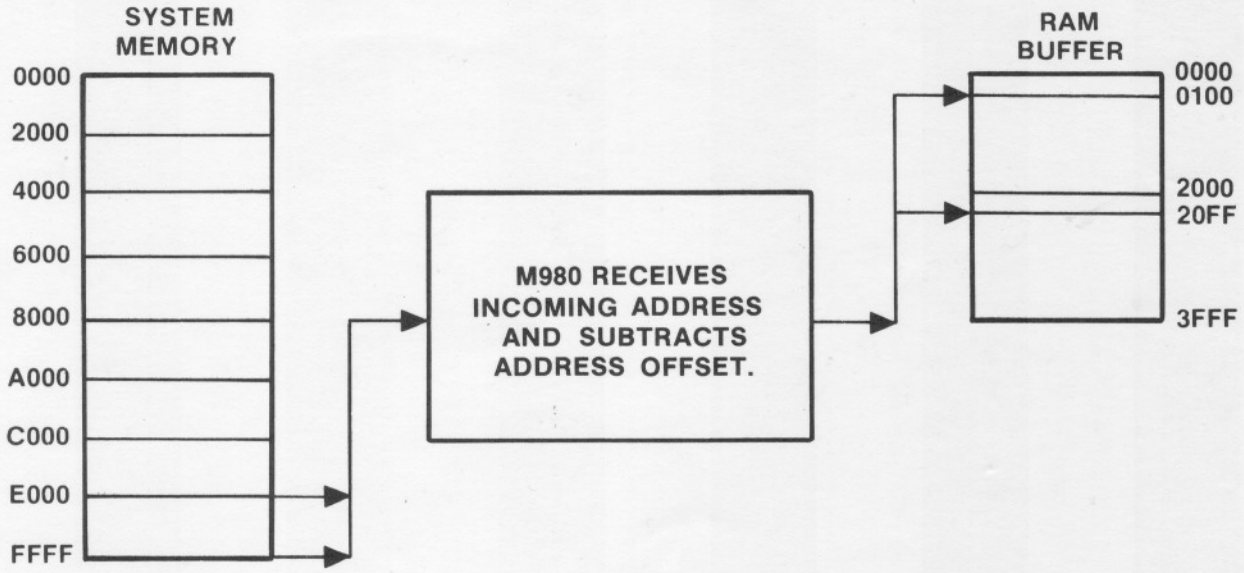


Figure 20-3E. Downloading.

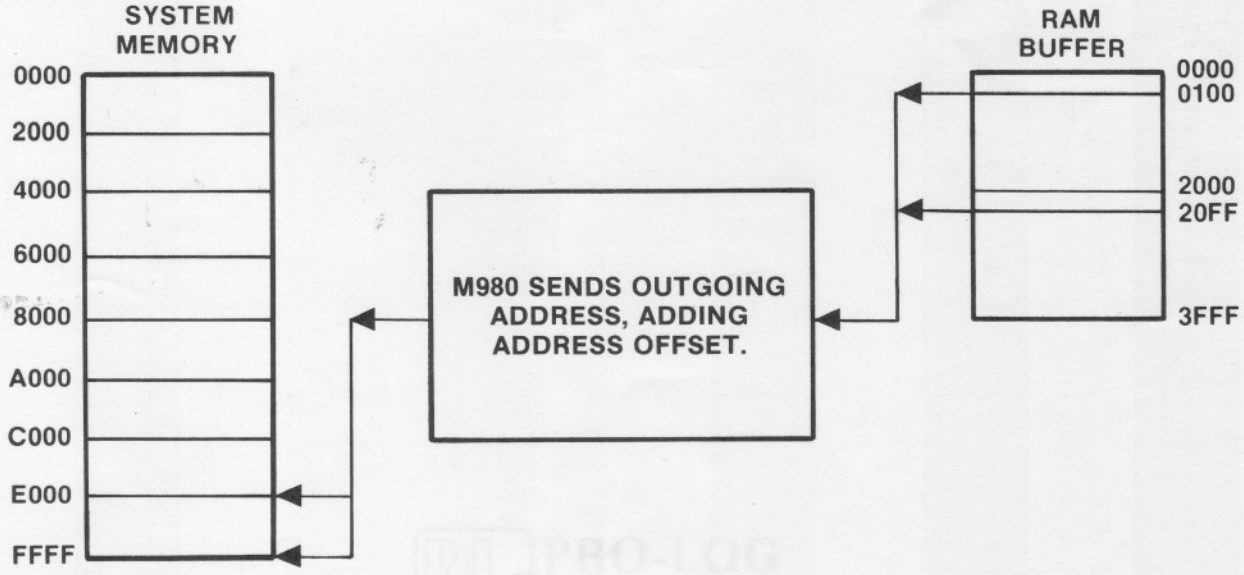
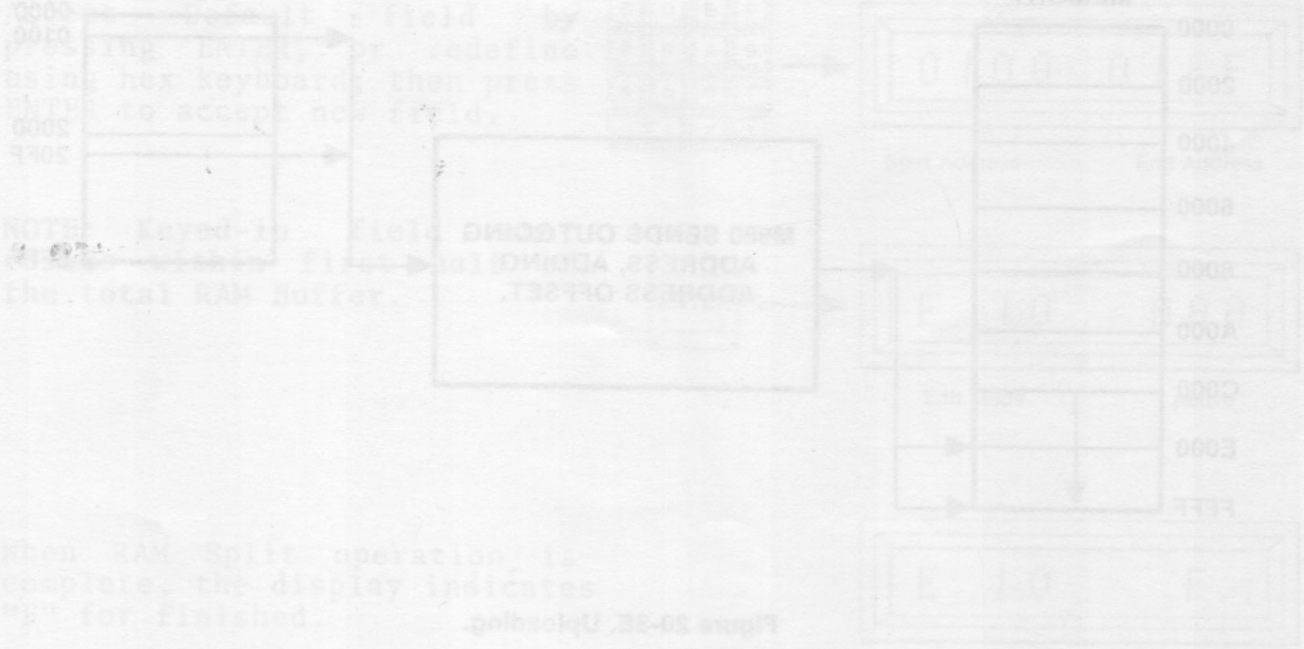


Figure 20-3E. Uploading.



INSERT ON PAGE 20-20 AFTER STEP 7

RS-232C 16K WRAPAROUND FEATURES OF M980 RAM BUFFER

In all RS-232C formats where the address information is presented with the incoming data stream (Intel, Motorola, Tek-Hex, etc.), the Absolute Addresses are accepted and wraparound occurs after the end of each 16K boundary is reached (i.e., addresses 3FFF, 7FFF, BFFF, and FFFF).

The M980 RAM Buffer is addressed with a 14-bit address bus. When the Absolute Address (16 bit) is received, the two high-order address bits are ignored. When 16K boundaries are crossed, the Buffer is addressed at location 0000 hex. For example: Absolute Address 4000 hex (0100 0000 0000 0000) addresses the buffer at address 0000 hex (0000 0000 0000 0000).

These bits are ignored by the M980

As a result, data wraparound occurs at 16K boundaries. If the buffer is less than 16K, data written to nonbuffered locations are lost.

M980 BUFFER SIZE CONSIDERATIONS

16K RAM Buffer: All absolute addresses and their associated data are accepted and wraparound occurs after addresses 3FFF, 7FFF, BFFF, and FFFF (see Fig. 20-5A).

8K RAM Buffer: Only absolute addresses 0000 through 1FFF, 4000 through 5FFF, 8000 through 9FFF, and C000 through DFFF are accepted. All other absolute addresses and their data are lost (see Fig. 20-5B).

4K RAM BUFFER: Only absolute addresses 0000 through 0FFF, 4000 through 5FFF, 8000 through 8FFF, and C000 through CFFF are accepted. All other absolute addresses and their data are lost (see Fig. 20-5C).

DOWNLOADING DATA FROM A DEVELOPMENT SYSTEM

When downloading data to the M980 from a development system, in which the program being downloaded is located in absolute addresses not available in the M980 RAM Buffer, the following procedure applies:

1. Move the program from its present memory locations to start at a memory location located on a 16K boundary. The 16K boundaries are located at addresses 0000, 4000, 8000, and C000. As an alternative, use the address offset procedure on page 20-3A.

2. Download the program to the M980, making sure that no more data is downloaded than the M980 RAM Buffer size can accommodate.

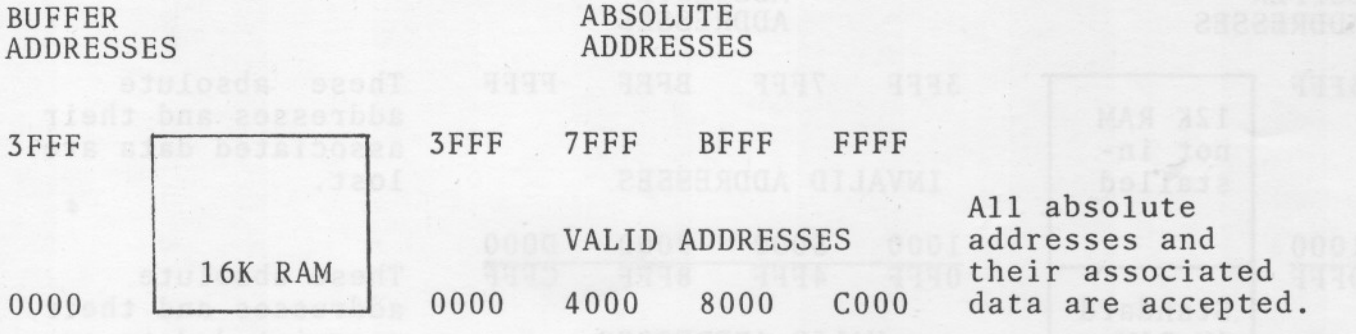


Figure 20-5A Example of 16K RAM Buffer and the Addresses Accepted as Valid Addresses for Loading Data

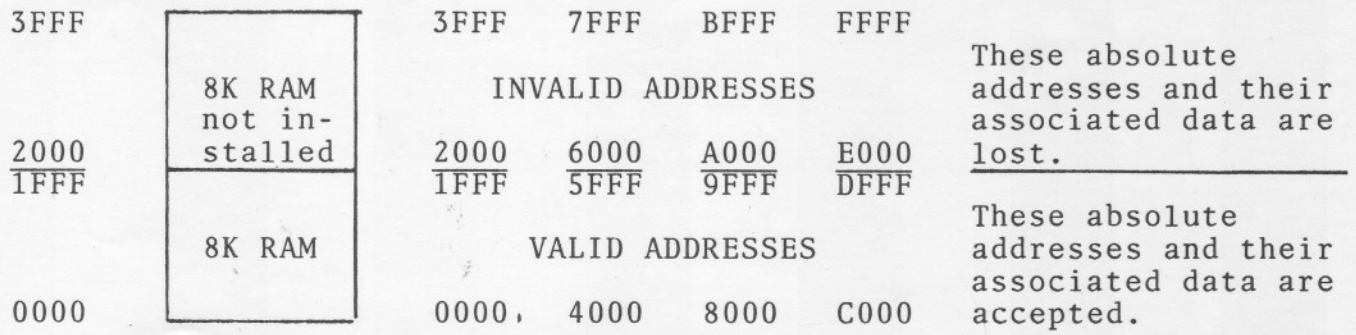


Figure 20-5B Example of 8K RAM Buffer and the Addresses Accepted as Valid Addresses for Loading Data

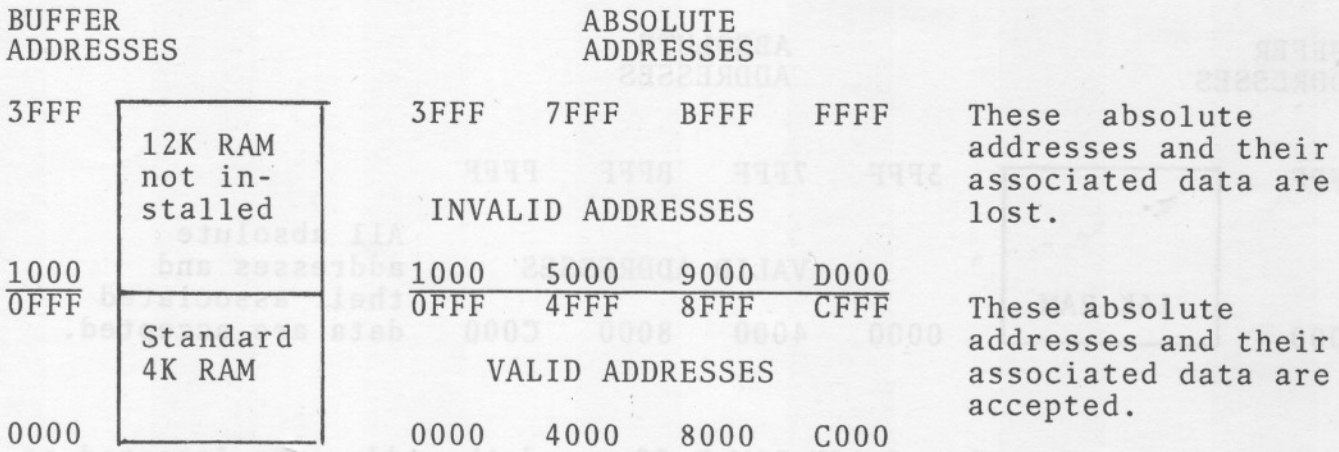


Figure 20-5C Example of 4K RAM Buffer and the Addresses Accepted as Valid Addresses for Loading Data

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